Asymmetrical Triangular Current Mode (ATCM) for Bidirectional High Step Ratio Modular Multilevel Dc–Dc Converter

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***Abstract*—Direct current (Dc) networks have proven advantages in high voltage direct current (HVDC) transmission systems, and now they are expanding to medium- and low-voltage distribution networks. One of the major challenges is to develop reliable dc–dc voltage transformation achieving high efficiency and performance, especially at high voltage and high step ratio. New resonant modular multilevel topologies have arisen as an alternative, mainly because of advantages such as optional use of transformers, natural voltage balance, simple control, and soft-switching capability. However, this type of operation generates a high peak current, does not allow control of power flow in all power range, and has a limited range of voltage variation. This article proposes an asymmetrical triangular current mode applied to high step ratio modular multilevel dc–dc converters. The proposed modulation increases the efficiency and achieves bidirectional control of the power, soft-switching, and a natural balance of the voltage in the cell capacitors. The experimental results show the bidirectional operation and the capacitor voltage balance of the converter under different operating conditions with higher efficiency (97.72%) and lower peak current compared to previous reports of this topology using resonant operation.**

***Index Terms*—Dc–dc conversion, high step ratio conversion, modular multilevel converter (MMC), triangular current mode (TCM).**

I. Introduction

DIRECT current (dc) has important advantages over alternating current (ac) in the transmission of electrical energy, such as lower power losses, less and smaller cables, and absence of reactive power nor peak voltages. However, these advantages have not been enough for the massive implementation of dc power systems due to the lack of competitive dc technology, especially high voltage dc–dc converters. The exception is the mature current source converter for high voltage direct current (HVDC) systems, which has demonstrated to be an economically and technically attractive option, mostly in specific point-to-point transmission systems such as offshore wind farms and long transmission lines [1]. Nowadays, the voltage source converter (VSC) in HVDC systems has arisen with the use of the modular multilevel converter (MMC) [2], because it introduces the capability to compensate reactive power, ac voltage control, black-start functionality, and multiterminal connection allowing large meshed and radial HVDC networks [3], [4]. On the other hand, the development of medium- and low-voltage direct current (MVDC–LVDC) networks is also of great interest due to the increase in dc loads and dc generation sources such as photovoltaic solar panels, electric vehicles, and battery energy storage systems. In this scenario, the dc–dc conversion that allows the interconnection of HVDC, MVDC, and LVDC systems is a key element for the development of the networks of the future.

A dc–dc converter for HV and MV range should provide high efficiency, bidirectional power flow, voltage regulation, and fault blocking capability [5], [6]. Several dc–dc converter topologies have been proposed, but there are two converter technologies that stand out for their high reliability, modularity, and flexibility: the input-series output-parallel converters, based on dc–dc building blocks [7]–[12]; and the modular multilevel front-to-front (MMC-FTF) converters [13]–[19].

The MMC-FTF uses two MMCs connected through a transformer and operates at a medium frequency to reduce the size of the transformer and the passive elements of the converter [14]. This solution provides full bidirectional power flow control and galvanic isolation, but it requires a complex voltage control and hard-switching operation that reduce efficiency, especially in high step ratio voltage transformation.

To solve this problem, resonant MMC topologies have been proposed for high step voltage ratio [20]–[23], adding soft-switching operation to decrease the power losses. These proposals used a resonant tank formed by the capacitors of the cells, which is excited by a square wave voltage at the resonant frequency, achieving zero-current-switching (ZCS) in the

Manuscript received July 7, 2019; revised October 16, 2019; accepted November 27, 2019. Date of publication December 3, 2019; date of current version March 13, 2020. This work was supported in part by the Chilean Research Council CONICYT under Grant FONDECYT 1171142, Grant FONDECYT Iniciacion 11190806, Grant SERC Chile (CONICYT/FONDAP/15110019), and under Grant CONICYT PFCHA/DOCTORADO BECAS CHILE/2019-21191912. This paper was presented at the IEEE Energy Conversion Congress & Expo 2018, September 17–23, 2018 in Portland, OR, USA. Recommended for publication by Associate Editor X. (GE) Ruan. *(Corresponding author: Cristian Pineda.)*

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Digital Object Identifier 10.1109/TPEL.2019.2957951

semiconductor devices. The voltage gain can be controlled changing the number of cells used in the stack modulation [21], [22], but it is more suitable for reconfiguration or for a degraded operation rather than for accurate voltage control due to its step behavior. Thus, control through the variation of the operating frequency has been the most employed technique [20], [24], allowing precise control of transferred power. However, operation at a frequency different than the resonant frequency is more complex to model and the ZCS is lost, limiting the power range in which the converter is highly efficient. Also, the resonant operation is highly sensitive to the parameters of the resonant tank, requires a design that carefully considers parasitic elements, and generates high peak current in the ac link. This high peak current causes high conduction losses and low efficiency despite its soft-switching capability.

Alternatively, triangular current mode (TCM) scheme applied to dual active bridge (DAB) dc–dc converters [25], [26] achieves bidirectional control of the power maintaining ZCS operation without resonance. Therefore, the design process and control scheme are simpler than resonant operation, extending high-efficiency operation to full power range. Also, the bidirectional operation using TCM has a symmetrical gain in both directions of the power flow. In the resonant case, it needs a symmetric resonant tank as PI type or T type *LCL/CLC* resonant tank to get a symmetric gain [27], [28]. However, TCM has not been applied in MMC topologies because it is not compatible in a single-pole configuration.

This article presents a new asymmetrical TCM (ATCM) for high step ratio dc–dc MMC, which achieves bidirectional power flow through a simple control law, maintains ZCS operation, reduces the peak current compared to resonant mode, and presents natural balance of the voltage in the cell capacitors without the need of complex control strategies [29]. The high step ratio dc–dc MMC topology is presented in Section II, the proposed modulation of the converter is described in Section III, and the dynamic balance of power is analyzed in Section IV. Finally, the simulation and experimental results are shown in Section V.

II. High Step Ratio Modular Multilevel Dc–Dc Converter

The topology of the high step ratio dc–dc MMC is shown in Fig. 1. The high-voltage port contains a stack of N half-bridge cells connected through an inductor to an active full-bridge converter, enabling the bidirectional control power flow between the high-voltage side (V_{HV}) and the low-voltage side (V_{LV}). A transformer could be optionally used between the inductor and the full bridge to provide galvanic isolation and a higher step ratio. Additionally, filters are connected in high-voltage and low-voltage sides to decrease voltage and peak current, but they are not considered in the analysis for simplicity.

The dynamic equations that describe the general operation of the converter consider the voltages at both side of the inductor v_{L1} and v_{L2} as is shown in (1) and (2). The voltage v_{L1} is the difference between the voltage V_{HV} and the voltage in the half-bridge stack v_{stack}. The voltage v_{stack} is the sum of all voltages in the half-bridge cells v_i, therefore it can be

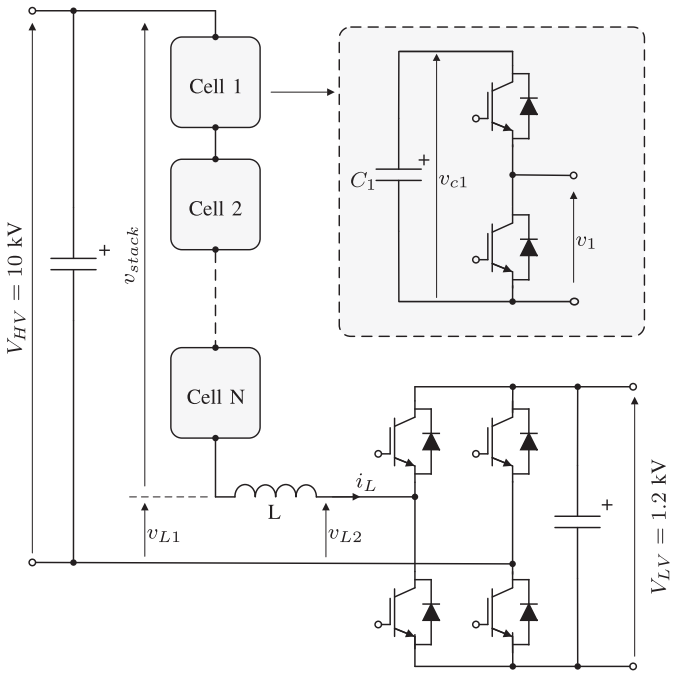

Fig. 1. Topology of the high step ratio dc–dc MMC using half-bridges in cells.

defined in terms of the commutation state $S_{i\text{-HB}} \in \{1, 0\}$ and the capacitor voltage v_{ci} of each cell ($v_{\text{stack}} = \sum_{i=1}^{N} v_{ci} \cdot S_{i\text{-HB}}$). On the other hand, the voltage v_{L2} is determined by the full-bridge commutation state $S_{\text{FB}} \in \{1, 0, -1\}$ and the low voltage V_{LV} ($v_{L2} = V_{\text{LV}} \cdot S_{\text{FB}}$). The inductor current i_L, the commutation state $S_{i\text{-HB}}$, and the capacitance C_i of each cell capacitor defines the capacitor voltage waveform v_{ci} in each half-bridge cell (2), determining their ripple, mean value, and dynamic behavior. The resistance r_{eq} represents the total conduction loss resistance in the converter generated by the inductor, switches, capacitors, and wire

$$L\frac{di_L}{dt} = \underbrace{V_{\text{HV}} - \overbrace{\sum_{i=1}^{N} v_{ci} \cdot S_{i-\text{HB}}}^{v_{\text{stack}}}}_{v_{L1}} - i_L \cdot r_{eq} - \underbrace{V_{\text{LV}} \cdot S_{\text{FB}}}_{v_{L2}} \quad (1)$$

$$C_i\frac{dv_{ci}}{dt} = i_L \cdot S_{i\text{-HB}}. \quad (2)$$

The inductor current i_L is controlled through the modulation of the voltages v_{L1} and v_{L2}, and the direction and magnitude of power are controlled directly with the inductor current.

III. Proposed Modulation Technique

The TCM requires a coordinated three-level voltage in both terminals of the inductor, v_{L1} and v_{L2}. The full-bridge generates three levels in v_{L2} by using unipolar modulation, but the stack requires a special modulation to get three levels in v_{L1}. Section III-A presents the proposed stack modulation. Then, Section III-B presents the TCM proposal.

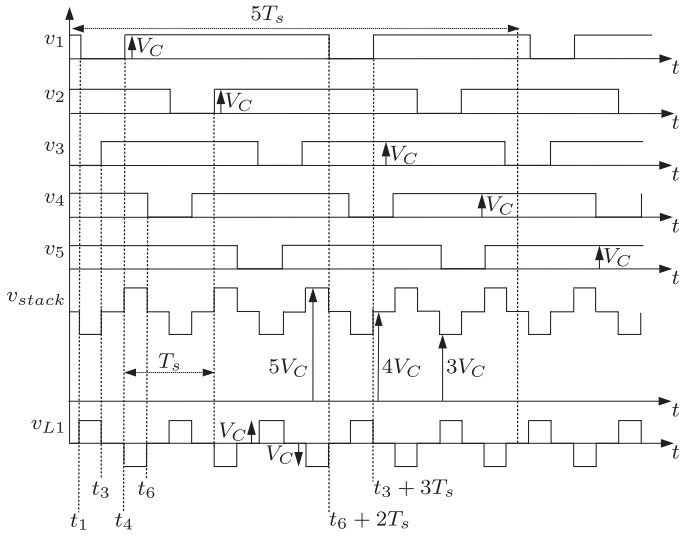

Fig. 2. Operation waves in high-voltage side for N = 5 cells and j = 2.

A. Half-Bridges Stack Modulation

The proposed modulation in the stack is aimed to generate a three-level voltage v_{L1} controlled by transitions times t_1, t_3, t_4, and t_6 as is shown in Fig. 2, extending the modulation presented in [23] to an asymmetric operation. In order to achieve this, the cells are modulated with the same waveform using a phase shift of T_S to reduce the resultant switching-frequency and to achieve a balanced use of the cells. The commutation state of the first half-bridge cell S_1^j is considered as a periodical signal of period $N \cdot T_s$ defined by transition times and a free parameter j as is shown in (3). j is a free parameter that defines a set of different cell waveforms in the half-bridge cell that cause the same voltage in the stack if $j \in \mathbb{N} \mid (0 \leq j < N-1)$

$$S_{1\text{-HB}}^j(t) = \begin{cases} 0 & \text{if } t_1 < t < t_4 \\ & t_6 + j \cdot T_s < t < t_3 + (j+1)T_s \\ 1 & \text{else} \end{cases}. \quad (3)$$

Therefore, a time-controlled voltage v_{stack} of three levels centered on $(N-1)V_C$, amplitude V_C, and period T_s is generated in the stack if the voltage in the cells are phase shifted by T_s and all the capacitor voltages in the cells are balanced and equal to V_C, as is determined below

$$v_{\text{stack}} = \begin{cases} & 0 < t < t_1 \\ (N-1)V_C & t_3 < t < t_4 \\ & t_6 < t < T_s \\ (N-2)V_C & t_1 < t < t_3 \\ N \cdot V_C & t_4 < t < t_6 \end{cases}. \quad (4)$$

Finally, a voltage v_{L1} of three levels centered on zero, amplitude V_C, period T_s and controlled by transition times t_1, t_3, t_4, and t_6 is obtained if the relation (5) is achieved, as is shown in (6)

$$V_C = \frac{V_{\text{HV}}}{(N-1)} \quad (5)$$

$$v_{L1} = \begin{cases} & 0 < t < t_1 \\ 0 & t_3 < t < t_4 \\ & t_6 < t < T_s \\ V_C & t_1 < t < t_3 \\ -V_C & t_4 < t < t_6 \end{cases}. \quad (6)$$

The proposed modulation waveforms for each cell is illustrated in Fig. 2, taking $N = 5$ and $j = 2$ as an example. The successful operation relies on all cells being healthy. However, in case of failure, it is possible to bypass the faulty cell and adjust the V_C to the new number of cells.

B. Asymmetrical Triangular Current Mode

Considering the stack modulation previously presented and neglecting the equivalent resistance r_{eq}, the dynamic equation (1) can be simplified to (7). This model is equivalent to a DAB linked by an inductor, allowing the use of the TCM [25]. TCM controls the power flow through the transition times of the voltages on both sides of the inductor. Therefore, the slope of the inductor current i_L is defined by the inductance L and its voltage, which is imposed by the difference between the voltages controlled by the stack v_{L1} and the full-bridge v_{L2} (7). The main advantages of the TCM are that it operates with soft-switching in most semiconductor transitions, and it can limit the peak current

$$L\frac{di_L}{dt} = v_{L1} - v_{L2}. \quad (7)$$

Conventional TCM generates a symmetric current in the inductor, which is desired for DAB converters, but it is a problem for the proposed topology. A symmetric current would generate zero power flow from the high-voltage side because the stack is connected in series with the high-voltage dc-link. To solve this problem, an ATCM scheme is proposed to achieve bidirectional control of the power and to maintain the ZCS. The proposed ATCM scheme is illustrated in Fig. 3.

During the intervals $(0, t_1)$, (t_3, t_4), and (t_6, T_s), the voltages v_{L1} and v_{L2} are zero to keep the current i_L constant and equal to zero. In t_1, a cell in the stack is bypassed generating V_C voltage in v_{L1} while the full bridge is kept in zero state [see Fig. 3(a)]. The voltage V_C is, therefore, applied to the inductor, causing the current i_L to increase linearly. In t_2, the full-bridge imposes the low-voltage (V_{LV}) in v_{L2}, so the inductor voltage is defined by the difference of the voltages applied by both converters ($V_C - V_{\text{LV}}$). Therefore, the low-voltage V_{LV} must be greater than V_C in order to obtain a negative slope of the inductor current and get ZCS at t_3. When the current reaches zero in t_3, an additional cell module is connected generating zero voltage in v_{L1} and the full bridge is switched applying zero voltage in v_{L2}. Thus, the equations for current i_L in a positive power flow are shown

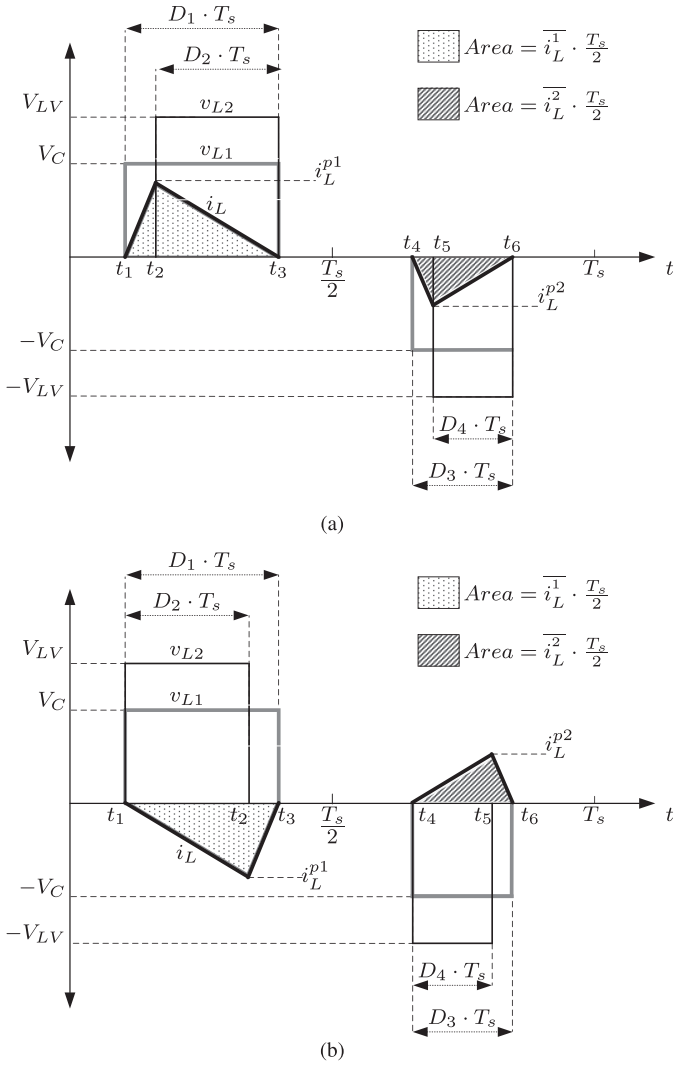

Fig. 3. Current and voltage waveforms for converter under ATCM and ZCS. (a) Power flow from high-voltage side to low-voltage side. (b) Power flow from low-voltage side to high-voltage side.

below

$$i_L(t) = \begin{cases} 0 & \text{if } t \in (0, t_1), (t_3, t_4) \\ & \vee (t_6, T_s) \\ \frac{V_C}{L}(t\text{–}t_1) & \text{if } t \in (t_1, t_2) \\ i(t_2) - \frac{V_{LV} - V_C}{L}(t\text{–}t_2) & \text{if } t \in (t_2, t_3) \\ -\frac{V_C}{L}(t\text{–}t_4) & \text{if } t \in (t_4, t_5) \\ i(t_5) + \frac{V_{LV} - V_C}{L}(t\text{–}t_5) & \text{if } t \in (t_5, t_6) \end{cases}. \quad (8)$$

ZCS restrictions are determined in (9) considering duty cycles D_i ($0 < D_i \leq 0.5$) as in Fig. 3(a), the conditions for continuity of the current i_L for t_2 and t_5 times, and imposing that the current reach zero in t_3 and t_6 times in (8)

$$D_{i+1} = \left(\frac{V_C}{V_{\text{LV}}}\right) D_i \qquad i = 1, 3. \quad (9)$$

Therefore, peak currents in the inductor i_L^{p1} and i_L^{p2} can be found in (10), using ZCS restrictions (9) and noticing that these occur in the t_2 and t_5 times

$$i_L^{p1} = i_L(t_2) = \frac{V_C}{f_s L}\left(1 - \frac{V_C}{V_{\text{LV}}}\right) D_1$$
$$i_L^{p2} = i_L(t_5) = -\frac{V_C}{f_s L}\left(1 - \frac{V_C}{V_{\text{LV}}}\right) D_3. \quad (10)$$

IV. Dynamic Balance of Power

The previous analysis requires that the mean voltage in the capacitors of the cells maintains a constant value during their operation. This section presents the voltage balance condition in the converter and a simple model to control the power transfer between ports maintaining this balance.

A. Voltage in the Cell Capacitors

Considering the ATCM and the proposed modulation, the voltage in each capacitor cell can be found integrating (2). The capacitor voltage at the end of the modulation time window $N \cdot T_s$ can be expressed using the peak currents as is shown below

$$v_{ci}(t_0 + N \cdot T_s) = v_{ci}(t_0) + \frac{i_L^{p1} \cdot (N-2) \cdot D_1 + i_L^{p2} \cdot N \cdot D_3}{2 f_s C_i}. \quad (11)$$

In order to achieve a steady-state balance in the voltage capacitors, this voltage must remain in the same value at the end of the modulation time window. Therefore, the steady-state voltage balance condition can be found below

$$D_3 = D_1 \sqrt{\frac{N-2}{N}}. \quad (12)$$

The ratio $\frac{D_3}{D_1}$ represents the level of asymmetry of the current in the inductor. Also, the asymmetry needed to keep the steady-state capacitors voltage balance decreases as the number of cells used increases.

The peak to peak voltage in the capacitors v_{ci}^{pp} in steady state depend of their capacitance, peak currents, and number of cells. Therefore, a capacitance value to keep the voltage ripple within a certain boundary can be obtained from (13) using the worse condition ($D_1 = 0.5$)

$$v_{ci}^{\text{pp}} = \frac{i_L^{p1} \cdot D_1 (N-2)}{N f_s C_i}. \quad (13)$$

B. Power Transfer

In order to calculate the power transferred between the high-voltage port, the low-voltage port, and the interchange of power among the cells, the average inductor currents in the first ($\overline{i_L^1}$) and second ($\overline{i_L^2}$) half cycles of the switching cycle are defined in (14) and illustrated in Fig. 3(a). These average currents can be defined as a function of the peak currents in the inductor i_L^{p1} and i_L^{p2} using the proposed ATCM, however, this analysis will

consider a generalized inductor current waveform at this point

$$\overline{i_L^{1}} = \frac{2}{T_s}\int_0^{\frac{T_s}{2}} i_L \cdot dt$$
$$\overline{i_L^{2}} = \frac{2}{T_s}\int_{\frac{T_s}{2}}^{T_s} i_L \cdot dt. \tag{14}$$

The average power delivered by the high-voltage port in one switching cycle P_{HV} is defined by the sum of the average currents $\overline{i_L^{1}}$ and $\overline{i_L^{2}}$ due to the inductor current waveform is the same as in the high voltage port if filters are not considered. On the other hand, the average power in the inductor P_{LV} is defined by its difference as is described in (15). The same capacitor voltage balance condition in the cell stack (12) is found through these equations considering ATCM and neglecting the power losses ($P_{\text{HV}} = P_{\text{LV}}$). This extends the voltage capacitor balance analysis to other modulations in the stack such as sorting modulation

$$\begin{bmatrix} P_{\text{HV}} \\ P_{\text{LV}} \end{bmatrix} = \begin{bmatrix} V_{\text{HV}} \\ V_C \end{bmatrix} \begin{bmatrix} \frac{1}{2} & \frac{1}{2} \\ \frac{1}{2} & -\frac{1}{2} \end{bmatrix} \begin{bmatrix} \overline{i_L^{1}} \\ \overline{i_L^{2}} \end{bmatrix}. \tag{15}$$

Alternatively, (15) can be expressed as a function of the average power for the stack P_{stack} in (16), because it is the difference of these two average power ($P_{\text{stack}}(k) = P_{\text{HV}} - P_{\text{LV}}$) if the cell power losses are neglected

$$\begin{bmatrix} P_{\text{HV}} \\ P_{\text{stack}} \end{bmatrix} = \begin{bmatrix} \frac{V_{\text{HV}}}{2} & \frac{V_{\text{HV}}}{2} \\ \frac{V_{\text{HV}}-V_C}{2} & \frac{V_{\text{HV}}+V_C}{2} \end{bmatrix} \begin{bmatrix} \overline{i_L^{1}} \\ \overline{i_L^{2}} \end{bmatrix}. \tag{16}$$

Thus, using (15) or (16), it is possible to control the power transfer between high-voltage and low-voltage ports through the average currents $\overline{i_L^{1}}$ and $\overline{i_L^{2}}$. The control law for the power flow P_{HV} is determined in (17), considering the ATCM lossless model in steady state. D_1 is able to control the power transfer and the maximum power $P_{\text{HV}}^{\text{max}}$ is obtained evaluating P_{HV} at $D_1 = 0.5$. A similar analysis can be performed for negative power flow inverting the phase shift of voltages v_{L1} and v_{L2} as is illustrated in Fig. 3(b). Therefore, these relationships allow full bidirectional control of the power flow while maintaining the ZCS and voltage balance in the converter

$$P_{\text{HV}} = \pm 4 D_1^2 P_{\text{HV}}^{\text{max}}$$
$$P_{\text{HV}}^{\text{max}} = \frac{(N-1)V_C^2(V_{\text{LV}} - V_C)}{4\, N f_s L \cdot V_{\text{LV}}}. \tag{17}$$

The resistive elements in the inductor (r_l), switches (r_{sw}), and capacitors (r_c) reduce the maximum power transfer due conduction losses and voltages drop at both sides of inductor. This voltage drop can be incorporated in the analysis of power transfer, considering the equivalent resistance r_{eq} as the sum of all resistance elements in the converter, as is shown in (18). Two switches in the full-bridge and N cell switches in the stack are conducting in any commutation state. Also, the number of capacitors connected can be approximated by a mean value of $(N-1)$ since the number of capacitors inserted using the proposed modulation is alternating between $(N-2), (N-1)$ and N

$$r_{\text{eq}} = r_l + (N+2)\cdot r_{\text{sw}} + (N-1)\cdot r_c. \tag{18}$$

Therefore, the power transfer considering voltage drop due resistive elements P_{HV}^{r} can be found solving

$$P_{\text{HV}}^{r} = \frac{D_1^2(N-1)V_C^2\left(V_{\text{LV}} - V_C - \frac{P_{\text{HV}}^{r}\cdot r_{\text{eq}}}{V_{\text{HV}}}\right)}{\left(N f_s L \cdot V_{\text{LV}} - \frac{P_{\text{HV}}^{r}\cdot r_{\text{eq}}}{V_{\text{HV}}}\right)}. \tag{19}$$

The main benefit of ATCM over the alternative resonant operation is a simpler model that works across the entire power range without losing ZCS. The resonant operation requires modifying the operating frequency to control the power transferred between the ports, making the model more complex and losing the ZCS at operating frequencies other than the resonant frequency. Alternatively, the ATCM model is valid in the entire power range with ZCS, making the converter highly efficient in any operation point. Also, the design process is easier and less restrictive due to the fixed frequency operation and the absence of the resonant tank highly dependent of parasitic elements or variations of cell capacitance.

The maximum peak current and stack voltage ratio ($\frac{v_{L1}^{\text{pp}}}{V_{\text{HV}}}$) are compared in Table I, showing a significant reduction in the maximum peak current for equivalent high voltage port and cells rate. However, ATCM generates less stack voltage ratio than the resonant operation because ATCM operates with three-levels voltage in the ac link instead of a two-level voltage. Therefore, the resonant operation achieves a higher voltage ratio at the same number of cells, meanwhile ATCM operates with better use of the dc current component.

TABLE I
RESONANT OPERATION AND ATCM COMPARISON

Parameter	Resonant Operation	ATCM
Maximum peak current	$\frac{\pi}{2}(2N-1+\frac{2}{\pi})\frac{P_{HV}^{max}}{V_{HV}}$	$2N\frac{P_{HV}^{max}}{V_{HV}}$
Stack voltage ratio	$\frac{2}{2N-1}$	$\frac{2}{N-1}$

V. RESULTS

This section presents two sets of results, the simulation in a 1-MW full-scale converter, and the experimental results in a scale-down prototype.

A. Real-Scale Simulation

The parameters of the full-scale proposed converter are listed in Table II. Different capacitance values are considered for each capacitor in the cells to evaluate the natural balance under more realistic conditions.

Fig. 4(a) shows the operation of the converter at 25% of the maximum power with the low-voltage side as load, illustrating

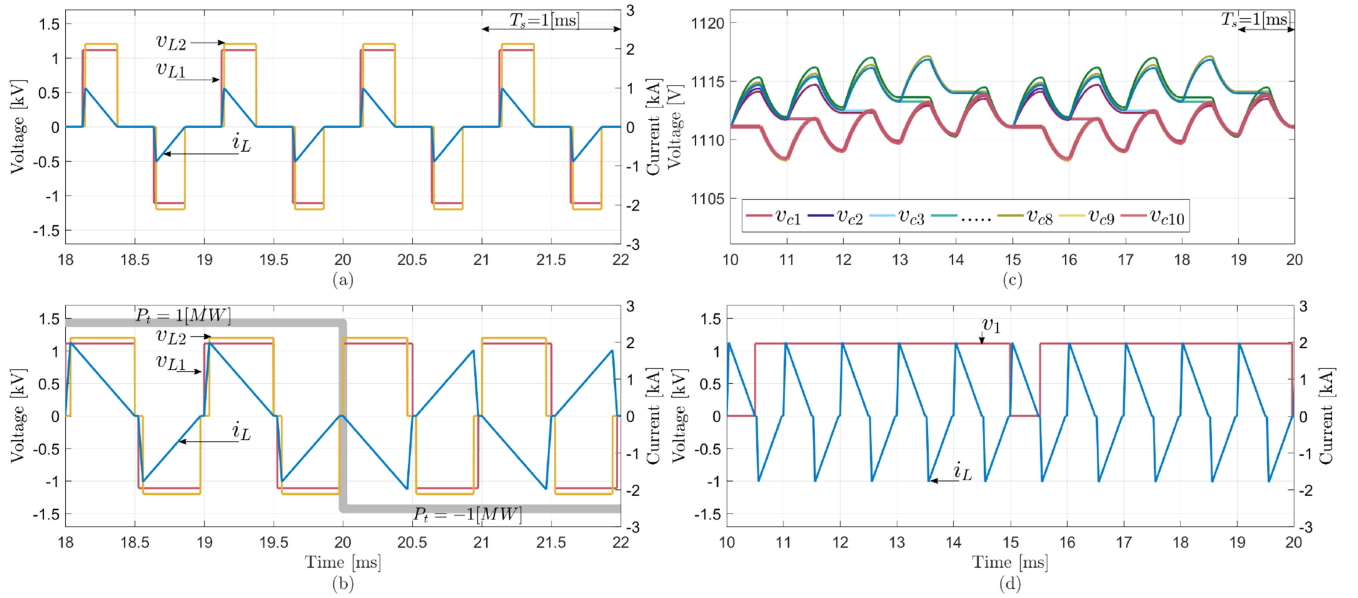

Fig. 4. Simulation waveforms. (a) Voltage and current at 25% of the maximum power. (b) Voltage and current for maximum power reversal. (c) Waveforms of capacitor cells voltages. (d) Voltage and current of one cell at maximum power.

TABLE II
PARAMETERS OF SIMULATION

Description	Parameter	Value
Maximum Power	P_{tmax}	1 MW
HV side Voltage	V_{HV}	10 kV
LV side Voltage	V_{LV}	1.2 kV
Number of cells	N	10
Inductor inductance	L	20.6 μH
Capacitance of cell capacitors	C_i	144 mF $\pm$ 20%
Switching frequency of the full-bridge	f_s	1 kHz
IGBTs ABB 5SNA3600E17000	V / I	1.7 kV / 3.6 kA

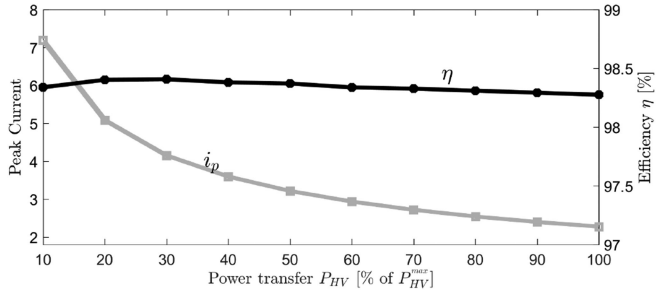

Fig. 5. Simulated power efficiency and peak current for different references of transfer power.

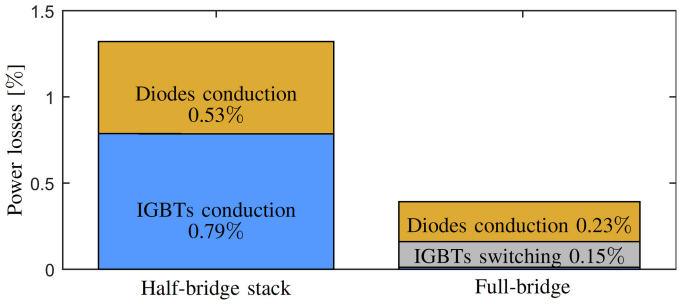

Fig. 6. Power losses distribution at full power transfer.

the voltages and current of the inductor in four switching periods. Fig. 4(b) illustrates the step response of the converter for maximum power reversal in the same time window.

The voltages of each cell capacitor in the modulation time window are shown in Fig. 4(c), verifying the correct power balance of the converter and cells even with different capacitance values for the capacitors of each cell. The ripple voltage in the capacitors is limited to 0.5% as it was designed.

Voltage and cell current for one cell are shown in Fig. 4(d), verifying the ZCS in this side of the converter. The voltage v_{c1} and v_1 represents the voltage of the capacitor and the output voltage of the cell one, respectively. Thus, the charge and discharge process of the capacitor v_{c1} can be observed in Fig. 4(c) and (d). Also, the ratio $\frac{N-2}{N}$ used in balance condition (12) can be deducted from Fig. 4(d) as the number of cycles of positive current over negative current in the cell while it is connected ($v_1 = V_C$).

The overall simulated efficiency is over 98.25% in all power ranges, as is shown in Fig. 5. The following power losses were taken into account: 1) IGBT conduction losses; 2) IGBT turn-on and turn-off switching losses; 3) diode reverse recovery losses; and 4) diode conduction losses. The power losses in the cells stack at full power represents 76.5% of total losses and are composed only by conduction losses due to the ZCS operation (see Fig. 6). The power losses in the low-voltage full-bridge at full power represent the other 23.5% of total losses and are distributed more evenly between conduction (59.6%) and switching losses (40.4%). The IGBTs switching losses in the full

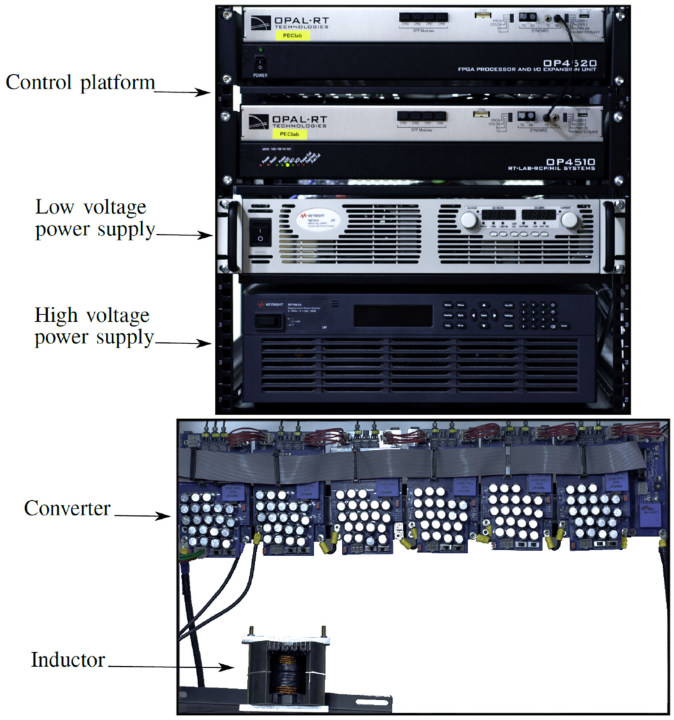

Fig. 7. Experimental scaled-down prototype.

bridge are generated by the only two hard-switching transitions at times t_2 and t_5, meanwhile the IGBT conduction losses are negligible because they are only conducting for the short periods (t_1, t_2) and (t_4, t_5) when the power flow is from high voltage to low voltage port [see Fig. 3(a)]. Thus, the full-bridge diodes are conducting most of the time, and their switching losses are almost zero because the transitions are made with ZCS at t_3 and t_6 times. The peak current is 2.27 times the average current at full power, and it increases as the power transfer decreases (see Fig. 5). Both efficiency and peak current achieve better results with ATCM than those previously presented using a resonant operation for a similarly designed converter [20].

B. Experimental Scale-Down Prototype

The scale-down prototype (see Fig. 7) was designed for 1.3 kW of maximum power transfer between a high-voltage side of 950 V and a low-voltage side of 260 V. The high voltage port was generated by a bidirectional dc power supply and the low voltage port by a unidirectional dc power supply, therefore the steady-state experiments consider a power flow from low- to high-voltage sides due the unidirectional power supply limitation. Predesigned cells were used in the stack, so the device technology (MOSFET) and the sizing are not optimal. IGBTs are a better option at this operating frequency because their lower conduction losses take advantage of the ZCS operation. However, the prototype works correctly to validate the theoretical analysis. The inductor was built using a ferrite core, and it was designed to avoid saturation in the core for a maximum peak current of 13 A. The detailed parameters of the prototype

TABLE III
PARAMETERS OF EXPERIMENTAL PROTOTYPE

Description	Parameter	Value
Maximum Power	P_{tmax}	1.3 kW
HV side Voltage	V_{HV}	950 V
LV side Voltage	V_{LV}	260 V
Number of cells	N	5
Inductor inductance	L	480 μH
Capacitance of cell capacitors	C_i	987 μF $\pm$ 20%
Switching frequency of the full-bridge	f_s	1 kHz
MOSFETs Infineon IPW65R041CFD	V / I	650 V / 80 A

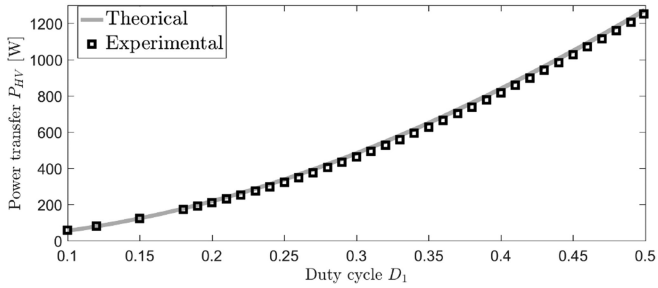

Fig. 8. Experimental power transfer versus duty cycle D_1.

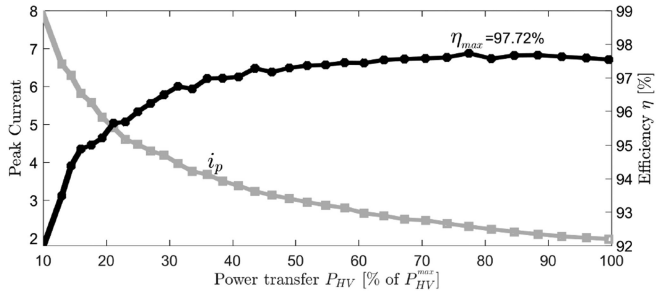

Fig. 9. Experimental power efficiency and peak current for different references of transfer power.

are listed in Table III. An OPAL-RT OP4510/4520 was used as the control platform and to generate the switching signals.

To validate the model, the converter was tested in the full range of power transfer. The experimental results validate the control of the power transfer through the duty cycle D_1 fitting well to the theoretical model considering the conduction losses from (19) as is shown in Fig. 8. The steady-state waveforms of voltages and current in the inductor at 25% of power transfer from low- to high-voltage ports show a behavior concordant with the previous theoretical analysis and simulations, as is illustrated in Fig. 10(a). The step response of the converter, from 210 W low- to high-side power transfers to 125 W high- to low-sides power [see Fig. 10(b)], demonstrates the fast response and the bidirectional capacity of the converter. However, the reference step should occur at the end of the switching time to avoid undesired transients in the inductor current, generating a delayed response by T_s at worst case.

The charge and discharge process of the cell capacitors can be observed in Fig. 10(c), validating the voltage balance in the

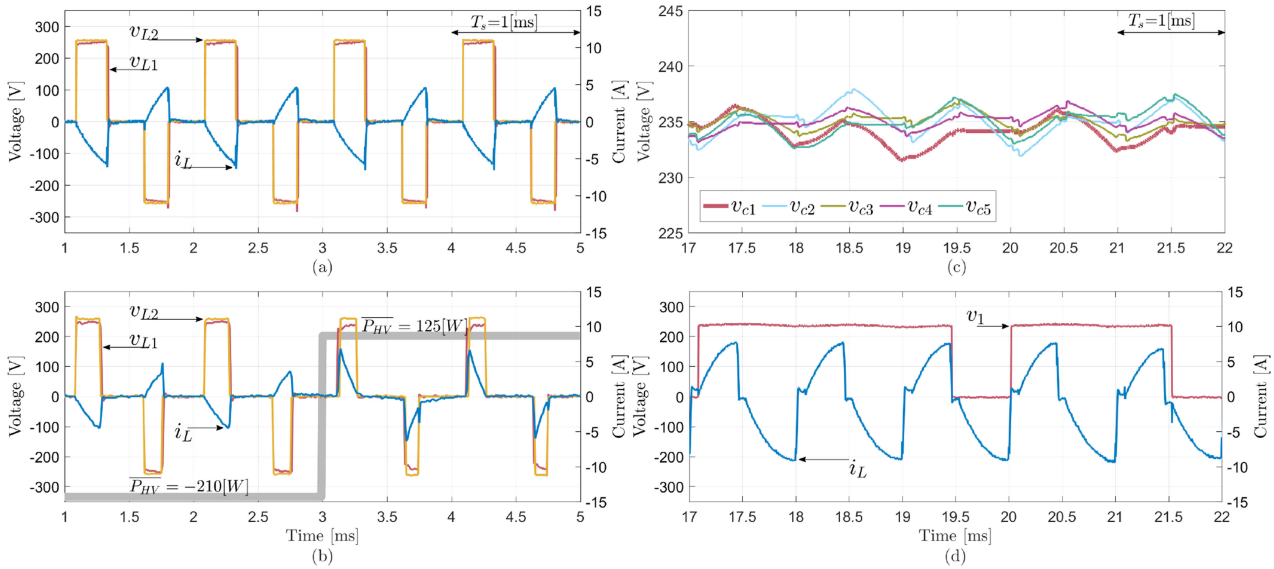

Fig. 10. Experimental waveforms. (a) Voltage and current at 25% of the maximum power from low voltage to high-voltage side. (b) Voltage and current for power reversal. (c) Waveforms of capacitor cells voltages at maximum power. (d) Voltage and current of one cell at maximum power.

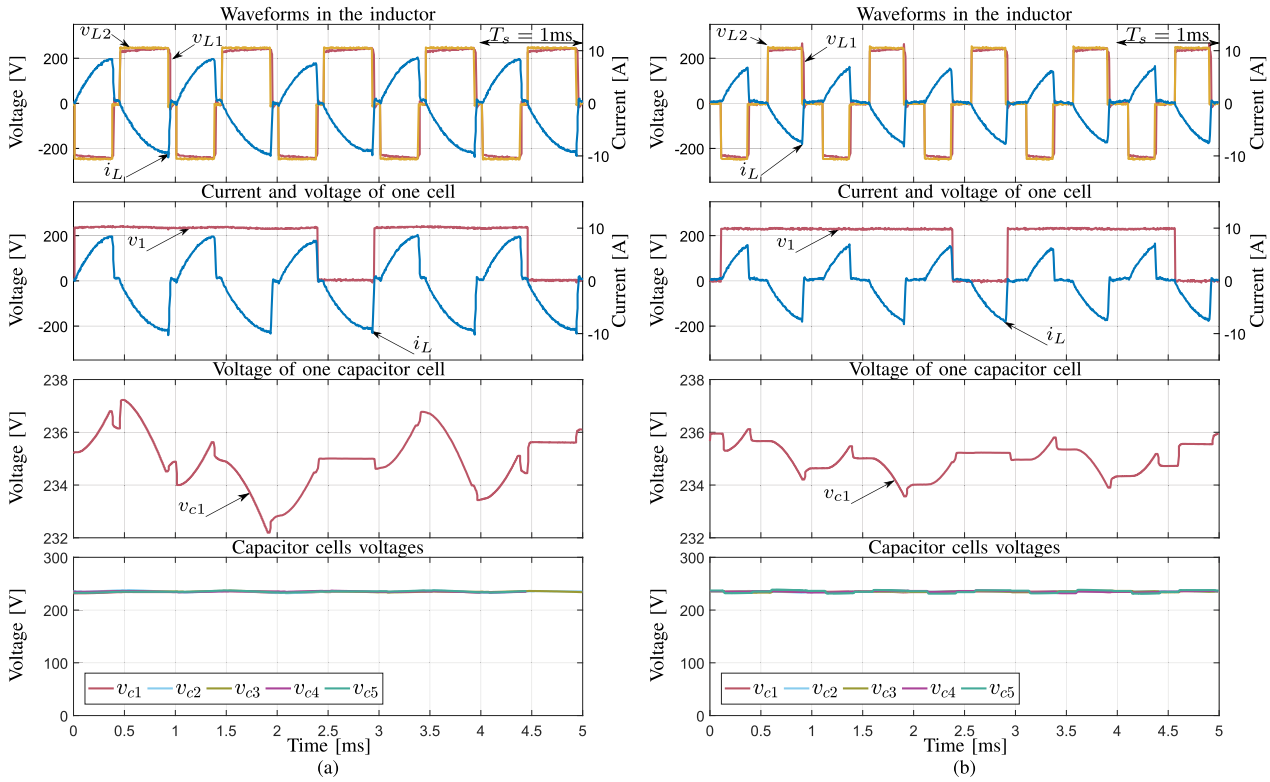

Fig. 11. Detailed experimental waveforms. (a) Waveforms at maximum power from low voltage to high voltage side. (b) Waveforms at 50% of maximum power from low-voltage to high-voltage sides.

capacitors using the proposed operation. The ripple voltage in the capacitors is 1.6% at this operation point validating the design equation (13).

Voltage and current of one cell in the modulation time window are shown in Fig. 10(d), verifying the soft-switching in the stack using the ATCM. The ratio of $\frac{N-2}{N}$ used in power balance condition is confirmed in this figure in the same way that was explained in the simulation section.

Detailed experimental waveforms at full power ($D_1 = \frac{1}{2}$) are illustrated in Fig. 11(a), showing the voltages and current in the inductor, the current and voltage of one cell, and all capacitor cell voltages. The same waveforms at 50% of maximum power

($D_1 = \sqrt{\frac{1}{8}}$) are shown in Fig. 11(b), allowing the comparison between these two points of operation. In both cases, the experimental results validate the previous analysis for waveforms in the inductor, ZCS in half-bridge cells, capacitor voltage ripple, and power balance.

The maximum efficiency of the prototype was 97.72% at 77% of maximum power transfer, and it remains over 97% in the 40–100% power transfer range as is shown in Fig. 9. At lower power transfer levels, the experimental efficiency decreases to a minimum of 92% because the losses independent of the power, such as those of the embedded measuring sensors, are increasingly relevant at lower power transfer levels. The experimental peak current is 1.98 times the average current at full power, and it increases as the power transfer decreases (gray line in Fig. 9) drawing a curve similar to the simulated in Fig. 5.

VI. Conclusion

An ATCM for a dc–dc MMC has been successfully validated, achieving bidirectional power control, ZCS, and balance of the voltage in capacitor cells. A simple control law is proposed to control the converter. Theoretical analysis has been verified with full-scale simulations and a scaled-down prototype, showing higher efficiency (97.72%) and lower peak current compared to previous reports of this topology using resonant operation. The experimental results confirm the operation principle, the voltage balance in the cells, and the operation at a high number of cells and voltages. As a disadvantage, the asymmetric operation in a dc–dc MMC with a low number of cells could saturate the core of the transformer if it is used for galvanic isolation. However, the asymmetry is reduced for high step ratio due to the need for a larger number of cells. With these results, the converter using ATCM has the potential to be a good solution for high step ratio dc–dc conversion.

References

[1] P. Bresesti, W. L. Kling, R. L. Hendriks, and R. Vailati, "Hvdc connection of offshore wind farms to the transmission system," *IEEE Trans. Energy Convers.*, vol. 22, no. 1, pp. 37–43, Mar. 2007.

[2] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech Conf. Proc.*, 2003, vol. 3, pp. 1–6.

[3] W. Hao, W. Dianfeng, and D. Pudney, "Hierarchical control in a 5-terminal vsc-hvdc project," *Energize*, p. 83, 2014.

[4] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.

[5] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge, and R. W. De Doncker, "Comparison of the modular multilevel dc converter and the dual-active bridge converter for power conversion in HVDC and MVDC grids," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 124–137, Jan. 2015.

[6] J. D. Páez, D. Frey, J. Maneiro, S. Bacha, and P. Dworakowski, "Overview of DC–DC converters dedicated to HVDC grids," *IEEE Trans. Power Del.*, vol. 34, no. 1, pp. 119–128, Feb. 2018.

[7] R. W. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high power density DC/DC converter for high power applications," in *Proc. IEEE Conf. Rec. Ind. Appl. Soc. Annu. Meet.*, 1988, pp. 796–805.

[8] W. Chen, X. Ruan, H. Yan, and K. T. Chi, "Dc/dc conversion systems consisting of multiple converter modules: stability, control, and experimental verifications," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1463–1474, Jun. 2009.

[9] G. Ortiz, "High-power DC-DC converter technologies for smart grid and traction applications," Ph.D. dissertation, ETH Zurich, Zurich, Switzerland, 2014.

[10] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y. R. De Novaes, "Isolated dc/dc structure based on modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 89–98, Jan. 2015.

[11] A. Mohammadpour, L. Parsa, M. H. Todorovic, R. Lai, R. Datta, and L. Garces, "Series-input parallel-output modular-phase dc–dc converter with soft-switching and high-frequency isolation," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 111–119, Jan. 2016.

[12] B. Zhao, Q. Song, J. Li, Q. Sun, and W. Liu, "Full-process operation, control, and experiments of modular high-frequency-link dc transformer based on dual active bridge for flexible mvdc distribution: A practical tutorial," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6751–6766, Sep. 2016.

[13] N. Denniston, A. M. Massoud, S. Ahmed, and P. N. Enjeti, "Multiple-module high-gain high-voltage dc–dc transformers for offshore wind energy systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1877–1886, May 2011.

[14] T. Lüth, M. M. Merlin, T. C. Green, F. Hassan, and C. D. Barker, "High-frequency operation of a dc/ac/dc system for hvdc applications," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4107–4115, Aug. 2014.

[15] J. A. Ferreira, "The multilevel modular dc converter," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4460–4465, Oct. 2013.

[16] K. Filsoof and P. W. Lehn, "A bidirectional modular multilevel dc–dc converter of triangular structure," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 54–64, Jan. 2015.

[17] I. Gowaid, G. Adam, A. M. Massoud, S. Ahmed, D. Holliday, and B. Williams, "Quasi two-level operation of modular multilevel converter for use in a high-power dc transformer with dc fault isolation capability," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 108–123, Jan. 2015.

[18] R. Vidal-Albalate *et al.*, "A modular multi-level dc-dc converter for hvdc grids," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc.*, 2016, pp. 3141–3146.

[19] S. Cui, N. Soltau, and R. W. De Doncker, "A high step-up ratio soft-switching dc–dc converter for interconnection of mvdc and hvdc grids," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2986–3001, Apr. 2018.

[20] X. Zhang, T. C. Green, and A. Junyent-Ferré, "A new resonant modular multilevel step-down dc–dc converter with inherent-balancing," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 78–88, Jan. 2015.

[21] Y. Li, X. Lyu, and D. Cao, "A zero-current-switching high conversion ratio modular multilevel dc–dc converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 151–161, Mar. 2017.

[22] X. Xiang, X. Zhang, G. P. Chaffey, and T. C. Green, "An isolated resonant mode modular converter with flexible modulation and variety of configurations for mvdc application," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 508–519, Feb. 2018.

[23] X. Zhang, M. Tian, X. Xiang, J. Pereda, T. C. Green, and X. Yang, "Large step ratio input-series-output-parallel chain-link dc-dc converter," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4125–4136, May 2018.

[24] D. Jovcic, "Bidirectional, high-power dc transformer," *IEEE Trans. Power Del.*, vol. 24, no. 4, pp. 2276–2283, Oct. 2009.

[25] G. Ortiz, H. Uemura, D. Bortis, J. W. Kolar, and O. Apeldoorn, "Modeling of soft-switching losses of IGBTs in high-power high-efficiency dual-active-bridge DC/DC converters," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 587–597, Feb. 2013.

[26] F. Jauch and J. Biela, "Generalized modeling and optimization of a bidirectional dual active bridge dc-dc converter including frequency variation," *IEEJ J. Ind. Appl.*, vol. 4, no. 5, pp. 593–601, 2015.

[27] A. Hillers, D. Christen, and J. Biela, "Design of a highly efficient bidirectional isolated LLC resonant converter," in *Proc. 15th Int. Power Electron. Motion Control Conf. Expo.*, 2012, vol. 1, pp. DS2b.13-1–DS2b.13-8.

[28] X. Tan and X. Ruan, "Equivalence relations of resonant tanks: A new perspective for selection and design of resonant converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2111–2123, Apr. 2016.

[29] C. Pineda, J. Pereda, X. Zhang, and F. Rojas, "Triangular current mode for high step ratio modular multilevel dc-dc converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 5185–5189.

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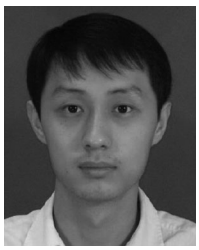

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